310404

Roll No. [redacted]

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B. Tech. III Sem. (Main) Exam., Dec. - 2019

Common for CS/IT

3CS3-04 Digital Electronics

Time: 3 Hours **Maximum Marks: 120**

Instructions to Candidates:

Part – A: *Short answer questions (up to 25 words) 10 ×2 marks = 20 marks. All ten questions are compulsory.*

Part – B: *Analytical/Problem Solving questions 5 ×8 marks = 40 marks. Candidates have to answer five questions out of seven.*

Part – C: *Descriptive/Analytical/Problem Solving questions 4 ×15 marks = 60 marks. Candidates have to answer four questions out of five.*

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting materials is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART - A

Q.1 Perform the following addition in excess – 3 code – [2]

(a) $(9)_{10} + (6)_{10}$ (b) $(168)_{10} + (234)_{10}$

Q.2 What is the advantage of using gray code? [2]

Q.3 Discuss De – Morgan Theorem? [2]

Q.4 Design NAND gate & Ex – Or gate using 2 – input NOR gate. [2]

Q.5 What are the advantages & disadvantage of ECL family? [2]

Q.6 Define the figure of Merit? [2]

Q.7 What is difference between combination circuits & sequential circuits? [2]

Q.8 Explain with diagram & truth table the operation of 4:1 Mux. [2]

Q.9 What is difference between latches and flip – flops? [2]

Q.10 Explain the race – around condition in flip – flop. [2]

PART – B

Q.1 Prove that Excess-3 code is a self – complementing code. [8]

Q.2 Minimize the following expression using K – map. [8]

$Y = \sum m(1, 5, 6, 7, 11, 12, 13, 15)$

Q.3 Implement the following Boolean expression using 8:1 multiplexer: [8]

$f(A, B, C, D) = \overline{A}\,\overline{B}\overline{D} + ABC + \overline{B}CD + \overline{A}\,CD$

Q.4 Give the comparison between Totem – pole and open collectors output of TTL? [8]

Q.5 Implement the following Boolean function using 3:8 decoder and external gates. [8]

$f(A, B, C) = \sum (2, 4, 5, 7)$

Q.6 Design full subtractor. [8]

Q.7 Draw the circuit diagram of M-S JK Flip – flop using NAND gates and explain its working. [8]

PART – C

Q.1 Find the minimal expression for the following function using Quince – McCluskey method. [15]

$$f(P, Q, R, S) = \sum m(0, 1, 4, 6, 8, 9, 10, 12) + d(5, 7, 14)$$

Q.2 Design a full subtractor using half – subtractors. [15]

Q.3 Design a conversion to convert SR flip – flop to – [15]

(a) J K Flip – flop

(b) D – Flip – flop

Q.4 Compare Synchronous and Asynchronous sequential circuit. Design and implement MOD – 6 synchronous counter using T- flip – flop. [15]

Q.5 Explain the working of 3 - input TTL? [15]
